First Named Inventor	Frankie F. Roohparvar	COMMUNICATION REGARDING CERTIFICATE OF CORRECTION
Patent No.	6,873,564	
Issue Date	March 29, 2005	
Examiner Name	Trong Q. Phan	
Attorney Docket No.	400.006US02	

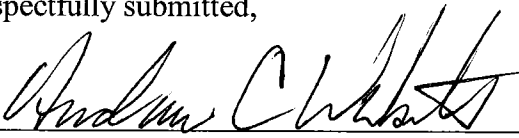| Title: ZERO LATENCY-ZERO BUS TURNAROUND SYNCHRONOUS FLASH MEMORY |
|---|

Attention Certificate of Corrections Branch
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Applicant hereby requests issuance of a Certificate of Correction in U.S. Letters Patent

No. 6,873,564 as specified on the attached four Certificates of Correction Forms (PTO/SB/44).

Applicant believes these corrections are necessary due to Applicant's errors of a clerical

nature and authorizes the payment of the $100.00 Certificate of Correction fee from Deposit

Account 501373. If deemed necessary, the U.S. Patent Office is authorized to charge any

additional fees found due to our Deposit Account No. 501373. Please contact the undersigned

attorney if you have any questions.

Respectfully submitted,

Date: 2/23/07

Andrew C. Walseth
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UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

Page __1__ of __4__

PATENT NO. : 6,873,564

APPLICATION NO.: 10/779,425

ISSUE DATE : March 29, 2005

INVENTOR(S) : Roohparvar

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 1, Line 47, delete "Many modem personal" and insert --Many modern personal--

Column 8, Line 8, delete Table 1:

TABLE 1

BURST DEFINITION

Burst Length	Starting Column Address			Type = Sequential (Order of Accesses Within a Burst)	Type = Interleaved
2			A0	0-1	0-1
			0	1-0	1-0
			1		
		A1	A0		
4		0	0	0-1-2-3	0-1-2-3
		0	1	1-2-3-0	1-0-3-2
		1	0	2-3-0-1	2-3-0-1
		1	1	3-0-1-2	3-2-1-0
8	A2		A1		
				0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
			A0	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0		0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
				3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
			0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	0		0	5-6-7-0-1-0-3-2	5-4-7-6-1-0-3-2
				6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
			1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0
	0		1		
			0		
	0		1		
			1		
	1		0		
			0		
	1		0		
			1		
	1		1		
			0		
	1		1		
			1		
Full Page 256	n= A0-A7 (location 0-255)			Cn, Cn + 1, Cn + 2 Cn + 3, Cn + 4 ... Cn - 1, Cn ...	Not supported

and insert Table 1:

TABLE 1

BURST DEFINITION

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2			A0	0-1	0-1
			0	1-0	1-0
			1		
4		A1	A0		
		0	0	0-1-2-3	0-1-2-3
		0	1	1-2-3-0	1-0-3-2
		1	0	2-3-0-1	2-3-0-1
		1	1	3-0-1-2	3-2-1-0
8	A2	A1	A0		
	0	0	0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0	0	1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0	1	0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0	1	1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1	0	0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1	0	1	5-6-7-0-1-0-3-2	5-4-7-6-1-0-3-2
	1	1	0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1	1	1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0
Full Page 256	n = A0-A7 (location 0-255)			Cn, Cn + 1, Cn + 2 Cn + 3, Cn + 4 ... Cn - 1, Cn ...	Not supported

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UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

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APPLICATION NO.: 10/779,425

ISSUE DATE : March 29, 2005

INVENTOR(S) : Roohparvar

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Columns 9 and 10, Line 33, delete Table 2:

TRUTH TABLE 2

Flash Memory Command Sequences

Operation	1st CYCLE					2nd CYCLE					3rd CYCLE				
	CMD	ADDR	ADDR	DQ	RP#	CMD	ADDR	ADDR	DQ	RP#	CMD	ADDR	ADDR	DQ	RP#
READ DEVICE Config.	LCR	90H	Bank	X	H	ACTIVE	Row	Bank	X	H	READ	CA	Bank	X	H
READ Status Register	LCR	70H	X	X	H	ACTIVE	X	X	X	H	READ	X	X	X	H
CLEAR Status Register	LCR	50H	X	X	H										
ERASE SETUP/ Confirm	LCR	20H	Bank	X	H	ACTIVE	Row	Bank	X	H	WRITE	X	Bank	D0H	H/V_{HH}
WRITE SETUP/ Confirm	LCR	40H	Bank	X	H	ACTIVE	Row	Bank	X	H	WRITE	Col	Bank	DIN	H/V_{HH}
WRITE Protect BLOCK/ Confirm	LCR	60H	Bank	X	H	ACTIVE	Row	Bank	X	H	WRITE	X	Bank	01H	H/V_{HH}
Protect DEVICE/ Confirm	LCR	60H	Bank	X	H	ACTIVE	X	Bank	X	H	WRITE	X	Bank	F1H	V_{HH}
Unprotect BLOCKS/ Confirm	LCR	60H	Bank	X	H	ACTIVE	X	Bank	X	H	WRITE	X	Bank	D0H	H/V_{HH}
ERASE NVmode Register	LCR	30H	Bank	X	H	ACTIVE	X	Bank	X	H	WRITE	X	Bank	C0H	H
WRITE NVmode Register	LCR	A0H	Bank	X	H	ACTIVE	X	Bank	X	H	WRITE	X	Bank	X	H
	R	H	k			VE	k				E	k			

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	CMD	ADDR	ADDR	DQ	RP #	CMD	ADDR	ADDR	DQ	RP #	CMD	ADDR	ADDR	DQ	RP #
READ DEVICE Config.	LCR	90H	Bank	X	H	ACTIVE	Row	Bank	X	H	READ	CA	Bank	X	H
READ Status Register	LCR	70H	X	X	H	ACTIVE	X	X	X	H	READ	X	X	X	H
CLEAR Status Register	LCR	50H	X	X	H										
ERASE SETUP/ Confirm	LCR	20H	Bank	X	H	ACTIVE	Row	Bank	X	H	WRITE	X	Bank	D0H	H/V$_{HH}$
WRITE SETUP/ WRITE	LCR	40H	Bank	X	H	ACTIVE	Row	Bank	X	H	WRITE	Col	Bank	DIN	H/V$_{HH}$
Protect BLOCK/ Confirm	LCR	60H	Bank	X	H	ACTIVE	Row	Bank	X	H	WRITE	X	Bank	01H	H/V$_{HH}$
Protect DEVICE/ Confirm	LCR	60H	Bank	X	H	ACTIVE	X	Bank	X	H	WRITE	X	Bank	F1H	V$_{HH}$
Unprotect BLOCKS/ Confirm	LCR	60H	Bank	X	H	ACTIVE	X	Bank	X	H	WRITE	X	Bank	D0H	H/V$_{HH}$
ERASE NV mode Register	LCR	30H	Bank	X	H	ACTIVE	X	Bank	X	H	WRITE	X	Bank	C0H	H
WRITE NV mode Register	LCR	A0H	Bank	X	H	ACTIVE	X	Bank	X	H	WRITE	X	Bank	X	H

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Column 22, Line 37, delete "After ERASE CONFIRM (DOH) is" and insert --After ERASE CONFIRM (D0H) is--

Column 24, Line 64, delete "A deep power-down mode is enable by" and insert --A deep power-down mode is enabled by--

Column 26, Line 15, delete "memory determines if nil blocks should" and insert --memory determines if all blocks should--

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